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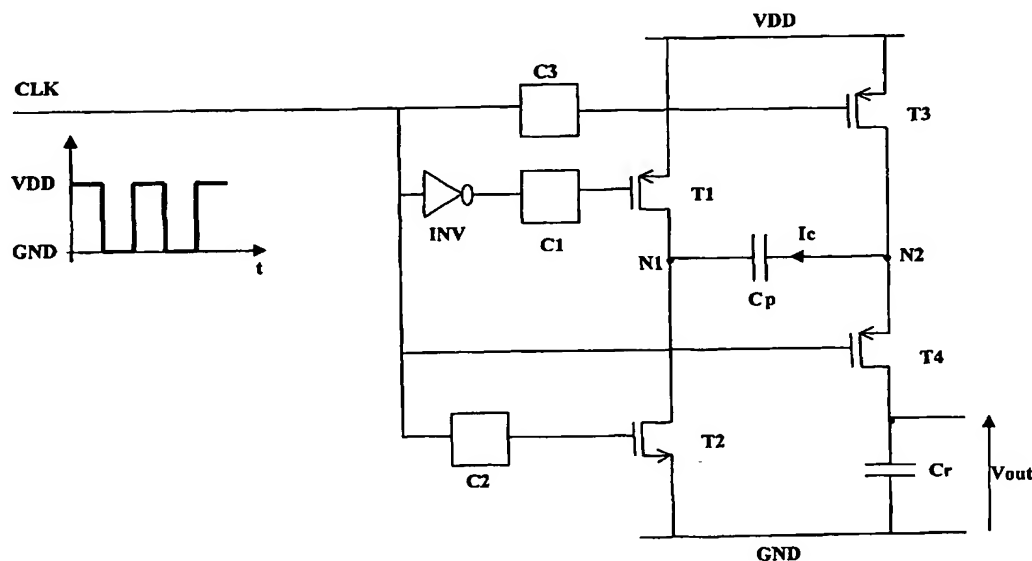
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(54) Title: **VOLTAGE CONVERTER USING MOS TRANSISTORS**

(57) **Abstract:** The invention relates to a voltage converter for generating an output voltage at an output terminal from an input voltage VDD taken from ground GND, said voltage converter comprising a switched capacitance Cp arranged in a bridge of transistors of the MOS type functioning as switches, each transistor being controlled by a control signal having a level varying in the rhythm of a clock signal clock. The invention is characterized in that the converter comprises at least a control circuit for supplying said control signal applied between the gate and the source of one of the transistors functioning as a switch, said control circuit having the particular function of generating a control signal having an amplitude which is inversely proportional to the input voltage VDD when the transistor which it controls is equivalent to a closed switch.

## Voltage converter using MOS transistors

## FIELD OF THE INVENTION

The invention relates to a voltage converter for generating an output voltage at an output terminal from an input voltage VDD taken from ground GND, said voltage converter comprising:

- 5 - a capacitance  $C_p$  having a first terminal N1 and a second terminal N2,
- four transistors T1-T2-T3-T4 of the MOS type functioning as switches, each transistor being controlled by a control signal having a level varying in the rhythm of a clock signal, each transistor comprising a source, a gate, a drain, and such that the first transistor T1 is connected between the input voltage VDD and the first terminal N1, the second transistor
- 10 T2 is connected between the first terminal N1 and ground GND, the third transistor T3 is connected between the input voltage VDD and the second terminal N2, and the fourth transistor T4 is connected between the second terminal N2 and the output terminal.

The invention finds numerous applications in electronic apparatus with voltage converters using MOS-type transistors.

15

## BACKGROUND OF THE INVENTION

Numerous electronic equipment having only one input voltage of a low level use a voltage converter with which an output voltage of a higher amplitude can be generated. Particularly, voltage doublers are currently used for multiplying the amplitude of the input

20 voltage by two.

Fig. 1 shows a prior-art voltage converter referred to as "switched capacity" converter. This is a voltage doubler.

This voltage converter uses four transistors T1-T2-T3-T4 functioning as switches, as well as a capacitance  $C_p$ . The transistors T2 and T3 are closed at the high levels of the clock signal CLK, while the transistors T1 and T4 are closed at the low levels of the

25 clock signal CLK via the inverter INV.

When T2 and T3 are equivalent to closed switches, the capacitance  $C_p$  is charged until it has a potential difference  $U_{cp} = VDD$  at its terminals. When T1 and T4 are, in their turn, equivalent to closed switches, the terminal N1 is connected to the input voltage

VDD which, taking the charge state of the capacitance  $C_p$  into account, brings the output terminal  $V_{out}$  to the potential  $2 \cdot VDD$ .

The capacitance  $C_r$  does not have an important role for the function of the converter but allows a reduction of the ripple of the output voltage.

5 This type of voltage converter has a certain number of limitations when the level of the input voltage varies from one electronic apparatus to another.

At different switching instants of the switches  $T2-T3$  and  $T1-T4$ , the capacitance  $C_p$  is charged with a time constant which is defined by the resistances of the drain-source junctions of the transistors  $T2-T3$  and  $T1-T4$ . The peaks of the switching current  
10  $I_c$  at different switching instants are therefore proportional to the input voltage  $VDD$  and inversely proportional to the resistance of the drain-source  $R_{MOS}$  of the transistors  $T2-T3$  and  $T1-T4$ . The switching current  $I_c$  thus has the form of:

$$I_c = K1 \cdot VDD / R_{MOS} \quad \text{with } K1 = \text{constant} \quad \text{Eq.1}$$

Moreover, when they are equivalent to closed switches, the resistance  $R_{MOS}$  of the transistors  
15  $T1-T2-T3-T4$  of the MOS type is inversely proportional to their gate-source voltage, i.e. inversely proportional to the input voltage  $VDD$  when they are equivalent to closed switches when a potential difference  $V_{GS0}$  of the amplitude  $VDD$  is applied between their gate and their source via the signal  $CLK$ . The resistance  $R_{MOS}$  of each transistor  $T1-T2-T3-T4$  is thus in the form of:

$$\begin{aligned} R_{MOS} &= K2 / V_{GS0} & \text{with } K2 = \text{constant} & \quad \text{Eq.2} \\ R_{MOS} &= K2 / VDD \end{aligned}$$

While taking Eq.1 into account, the switching current  $I_c$  increases in a quadratic manner as a function of the input voltage  $VDD$ . Consequently, it has the form of:

$$25 \quad I_c = K3 \cdot VDD^2 \quad \text{with } K3 = \text{constant} \quad \text{Eq.3}$$

These switching current peaks generate parasitic noise which is stronger as the amplitude of the peaks is higher. Particularly if the input voltage  $VDD$  increases from electronic equipment to electronic equipment, the parasitic noise also increases. Taking into account that the current  $I_c$  increases in a quadratic manner as a function of the input voltage  
30  $VDD$ , a small variation of the input voltage  $VDD$  involves a considerable variation of the switching current and thus of the parasitic noise.

With such a voltage converter, the noise level can therefore not be guaranteed at a constant level when the input voltage  $VDD$  varies, even if  $VDD$  varies only very slightly.

This technical limitation of such a prior-art converter is particularly annoying for satisfying the requirements of electromagnetic compatibility standards.

## OBJECT AND SUMMARY OF THE INVENTION

5 It is an object of the invention to provide a voltage converter with which the variations of the switching current can be reduced.

To this end, the voltage converter is characterized in that it comprises at least a control circuit for supplying said control signal applied between the gate and the source of one of the transistors T1-T2-T3 functioning as a switch, said control circuit having the  
10 particular function of generating a control signal having an amplitude which is inversely proportional to the input voltage VDD when the transistor which it controls is equivalent to a closed switch.

The control signal  $V_{GS}$  generated by the control circuit according to the  
15 invention has the form of:

$$V_{GS} = K4 / VDD \quad \text{with } K2 = \text{constant} \quad \text{Eq.4}$$

The resistance  $R_{MOS}$  of the transistor controlled by the control circuit has the form of:

$$R_{MOS} = K2 / V_{GS} \quad \text{with } K2 = \text{constant} \quad \text{Eq.5}$$

20

Taking Eq.4 and Eq.5 into account, the resistance  $R_{MOS}$  will be proportional to the input voltage VDD. The resistance  $R_{MOS}$  has the form of:

$$R_{MOS} = K5.VDD \quad \text{with } K5 = \text{constant} \quad \text{Eq.6}$$

25 Taking Eq.1 and Eq.6 into account, the switching current  $I_c$  will be invariant at the variations of the input voltage VDD. The switching current thus has the form of:

$$I_c = K6 \quad \text{with } K6 = \text{constant} \quad \text{Eq.7}$$

30 The variations of the peaks of the switching current  $I_c$  at different switching instants of the transistors T2-T3 and T1-T4 are thus canceled by generating a control signal having an amplitude which is inversely proportional to the input voltage VDD. The peaks of the switching current  $I_c$  are thus invariant with respect to the variations of the input voltage VDD, which guarantees a constant noise level when the input voltage VDD varies.

The invention is also characterized in that said control circuit comprises, when it controls a transistor of the P-MOS type:

- an additional transistor M1 of the P-MOS type functioning as a closed switch,
- a current source IREF\_1 arranged in series with the drain-source junction of said additional transistor M1,
- a switch COM1 having two inputs, the first input E1 of which is connected to the central tap P of the additional transistor M1 and the current source IREF\_1, and the second input E2 is connected to the input voltage VDD, said switch being controlled via said clock signal.

This association of means provides the possibility of generating, at low cost, a control signal having an amplitude which is inversely proportional to the input voltage VDD.

An additional advantage of this particular embodiment is the very good compensation of the variations of the resistance  $R_{MOS}$  of the additional transistor and the transistor controlled by the control circuit in so far as these transistors may be identical.

The invention is also characterized in that said control circuit comprises, when it controls a transistor of the N-MOS type:

- an additional transistor M2 of the N-MOS type functioning as a closed switch,
- a current source IREF\_2 arranged in series with the drain-source junction of said additional transistor M2,
- a switch COM2 having two inputs, the first input E1 of which is connected to the central tap P of the additional transistor M2 and the current source IREF\_2, and the second input E2 is connected to ground GND, said switch being controlled via said clock signal.

This association of means provides the possibility of generating, at low cost, a control signal having an amplitude which is inversely proportional to the input voltage VDD.

An additional advantage of this particular embodiment is the very good compensation of the variations of the resistance  $R_{MOS}$  of the additional transistor and the transistor controlled by the control circuit in so far as these transistors may be identical.

The invention also relates to an integrated circuit, comprising a voltage converter according to the invention.

The invention also relates to a device for reading smart cards comprising a voltage converter according to the invention for generating an output voltage having a higher amplitude from an input voltage. This output voltage is intended to serve as input voltage for

a voltage regulator supplying a set of output voltages for feeding a smart card, and thus provides the possibility of exchanging data between the reading device and the smart card.

## BRIEF DESCRIPTION OF THE DRAWINGS

5                   These and other aspects of the invention are apparent from and will be elucidated, by way of non-limitative example, with reference to the embodiment(s) described hereinafter.

                  In the drawings:

                  Fig. 1 shows a voltage converter of the prior art,

10                   Fig. 2 shows a voltage converter according to the invention,

                  Fig. 3 is a first control circuit for controlling transistors of the P-MOS type in a voltage converter according to the invention,

                  Fig. 4 is a second control circuit for controlling transistors of the N-MOS type in a voltage converter according to the invention,

15                   Fig. 5 shows a device for reading smart cards, comprising a voltage converter according to the invention.

## DESCRIPTION OF EMBODIMENTS

                  Fig. 2 shows a voltage converter according to the invention. This converter is based on the same operating principle as the prior-art voltage converter described with reference to Fig. 1.

                  To this end, the converter shown in Fig. 2 uses transistors T1-T2-T3-T4 of the MOS type functioning as switches. The transistors T1-T3-T4 are of the P-MOS type while the transistor T2 is of the N-MOS type.

25                   When the transistors T2-T3 are equivalent to closed switches, the transistors T1-T4 are equivalent to open switches. Inversely, when the transistors T2-T3 are equivalent to open switches, the transistors T1-T4 are equivalent to closed switches. The change of state of the transistors T1-T2-T3-T4 functioning as switches is effected in the rhythm of the clock signal CLK.

30                   The switching cycle of the transistors T1-T2-T3-T4 allows charging of the capacitance  $C_p$  when the transistors T2-T3 are equivalent to closed switches so as to supply an output voltage  $V_{out}$  having a level which is higher than the input voltage  $V_{DD}$  when the transistors T1-T4 are equivalent to closed switches.

The transistors T1-T2-T3 are controlled by control circuits according to the invention so as to allow a change of state of the transistors T1-T2-T3 functioning as switches by generating a control signal applied between the gate and the source of each transistor controlled in this way.

5           The control circuits C1 and C3 are identical because they control both transistors of the P-MOS type. The control circuit C1 controlling the transistor T1 supplies a control signal which varies in the rhythm of the inverse value of the clock signal CLK via the inverter INV, while the control circuit C3 supplies a control signal which varies in the rhythm of the clock signal CLK. The control circuit C2 dedicated to the control of a transistor of the  
10 N-MOS type supplies a control signal which varies in the rhythm of the clock signal CLK.

Each control circuit is characterized in that it supplies a control signal having an amplitude which is inversely proportional to the input voltage VDD when the transistor which it controls is equivalent to a closed switch. This has the result that the resistance  $R_{MOS}$  of each transistor controlled by the control circuit becomes proportional to the input voltage  
15 VDD. Consequently, the switching current  $I_c$  becomes invariant to the variations of the input voltage VDD.

Each control circuit thus provides the possibility of supplying said control signal at such a potential level that it enables the transistor which it controls to function as an open switch. To this end, the control signal has the level of the input voltage VDD if the  
20 controlled transistor is of the P-MOS type and has the level of ground GND if the controlled transistor is of the N-MOS type.

The capacitance  $C_r$  does not play a major role as regards the operating principle of the converter, but it allows a reduction of the ripple of the output voltage  $V_{out}$ .

The transistor T4 of the P-MOS type is directly controlled at its gate by the  
25 clock signal CLK in such a way that it is equivalent to a closed or an open switch at the same time as the transistor T1.

Although Fig. 2 shows a converter using a control circuit for each transistor T1, T2 and T3, the invention also provides a voltage converter (not shown) in which only one or two of the transistors T1, T2 and T3 are controlled by a control circuit. This converter  
30 provides the possibility of obtaining a converter at lower cost because the number of control circuits is reduced.

Fig. 3 is a first control circuit for controlling transistors of the P-MOS type in a voltage converter according to the invention.

Such a control circuit C1 is used for controlling the transistor T1 of the P-MOS type, and such a control circuit C3 is used for controlling the transistor T3 of the P-MOS type.

Each control circuit comprises an additional transistor M1 of the P-MOS type functioning as a closed switch. To this end, the gate of the transistor M1 is connected to ground GND so that a potential difference  $V_{GS0} = VDD$  is applied between the gate and the source of M1.

The control circuit also comprises a current source IREF\_1 arranged in series with the drain-source junction of said digital transistor M1. This current source supplies a current IREF\_1 in the drain-source junction of said additional transistor M1. The value of the current IREF\_1 is constant and is particularly independent of the input voltage VDD.

The control circuit also comprises a switch COM1 having two inputs E1 and E2, the first input E1 being connected to the central tap of the additional transistor and the current source, the second input E2 being connected to the input voltage VDD.

The switch COM1 is controlled by the clock signal CLK\_IN1. For the control circuit C1, the clock signal CLK\_IN1 corresponds to the clock signal supplied at the output of the inverter INV of Fig. 2. For the control circuit C3, the clock signal CLK\_IN1 corresponds to the clock signal CLK of Fig. 2.

When the clock signal CLK\_IN1 is at the low level, i.e. at ground GND, a potential VDD is applied to the gate of transistor T1/T3. The control circuit thus applies a potential difference  $V_{GS} = 0$  between the gate and the source of the transistor T1/T3. Consequently, the transistor T1/T3 is equivalent to an open switch.

When the clock signal CLK\_IN1 is at the high level, i.e. at the input voltage VDD, a potential  $V_{GS}$  which is equal to that at the central tap P between the current source IREF\_1 and the drain-source junction of M1 is applied to the gate of the transistor T1/T3. The control circuit thus applies a potential difference  $V_{GS}$  between the gate and the source of the transistor T1/T3, which is equal to the potential difference at the terminals of the drain-source junction of the transistor M1, which potential difference is inversely proportional to the input voltage VDD. Since the potential at the tap P has a small value, the potential difference  $V_{GS}$  has a value which is sufficiently high to render the transistor T1/T3 equivalent to a closed switch.

In other words, when such a control circuit controls a transistor of the P-MOS type equivalent to a closed switch, it provides the possibility of applying a potential  $V_G$  to the gate of the transistor T1/T3 which is slightly higher than ground GND by a quantity  $\epsilon$  (of



about several volts) so as to get rid of fluctuations of the input voltage VDD, in contrast to the prior-art converter in which a potential which is equal to GND would be applied to the gate of the transistor T1/T3.

5 In a particular embodiment, the inputs E1 and E2 of the switch COM1 of the switching circuit C1 are advantageously inverted in such a way that the clock signal CLK\_IN1 corresponds to the clock signal CLK, thus economizing on the inverter INV.

Fig. 4 shows a second control circuit for controlling transistors of the N-MOS type in a converter according to the invention.

10 Such a control circuit C2 is used for controlling the transistor T2 of the N-MOS type.

The control circuit C2 comprises an additional transistor M2 of the N-MOS type functioning as a closed switch. To this end, the gate of the transistor M2 is connected to the input voltage VDD so as to apply a potential difference  $V_{GS0} = VDD$  between the gate and the source of M2.

15 The control circuit also comprises a current source IREF\_2 arranged in series with the drain-source junction of said additional transistor M2. This current source supplies a current IREF\_2 in the drain-source junction of said additional transistor M2. The value of the current IREF\_2 is constant and is particularly independent of the input voltage VDD.

20 The control circuit also comprises a switch COM2 having two inputs E1 and E2, the first input E1 being connected to the central tap of the additional transistor and the current source, the second input E2 being connected to ground GND.

The switch COM2 is controlled by the clock signal CLK\_IN2. The clock signal CLK\_IN2 corresponds to the clock signal CLK of Fig. 2.

25 When the clock signal CLK\_IN2 is at the low level, i.e. at ground GND, a potential GND is applied to the gate of transistor T2. The control circuit thus applies a potential difference  $V_{GS} = 0$  between the gate and the source of the transistor T2. Consequently, the transistor T2 is equivalent to an open switch.

30 When the clock signal CLK\_IN2 is at the high level, i.e. at the input voltage VDD, a potential  $V_G$  which is equal to that of the central tap P between the current source IREF\_2 and the drain-source junction of M2 is applied to the gate of the transistor T2. The control circuit thus applies a potential difference  $V_{GS}$  between the gate and the source of the transistor T2, which is equal to the potential difference at the terminals of the drain-source junction of the transistor M2, which potential difference is inversely proportional to the input voltage VDD. Since the potential difference between the input voltage VDD and the tap P

has a small value, the potential difference  $V_{GS}$  has a value which is sufficiently high to render the transistor T2 equivalent to a closed switch.

In other words, when such a control circuit controls a transistor of the N-MOS type equivalent to a closed switch, it provides the possibility of applying a potential  $V_G$  to the gate of the transistor T2 which is slightly smaller than the input voltage VDD by a quantity  $\epsilon$  (of about several volts) so as to get rid of fluctuations of the input voltage VDD, in contrast to the prior-art converter in which a potential which is equal to VDD would be applied to the gate of the transistor T2.

Fig. 5 shows a device SCR for reading smart cards, comprising a voltage converter CONV according to the invention.

The device SCR comprises an input voltage source VDD connected to the input of a voltage converter according to the invention, as described with reference to Fig. 2. The converter CONV provides the possibility of supplying an output voltage  $V_{out}$  having a stronger amplitude than the input voltage VDD. Based on this output voltage  $V_{out}$ , a set of output voltages is generated by means of a voltage regulator REG, in which the regulation of these output voltages is effected on the basis of a reference voltage  $V_{ref}$  within the reading device SCR. Particularly, these output voltages have a level of 5 volts, 3 volts and 1.8 volts and are intended to feed a smart card SM communicating with the device SCR for the purpose of exchanging data DAT.

The voltage converter according to the invention can be advantageously integrated in an integrated circuit, particularly an integrated circuit dedicated to the management of a device for reading smart cards.

## CLAIMS:

1. A voltage converter for generating an output voltage at an output terminal from an input voltage VDD taken from ground GND, said voltage converter comprising:
    - a capacitance Cp having a first terminal N1 and a second terminal N2,
    - four transistors T1-T2-T3-T4 of the MOS type functioning as switches, each
  - 5 transistor being controlled by a control signal having a level varying in the rhythm of a clock signal, each transistor comprising a source, a gate, a drain, and such that the first transistor T1 is connected between the input voltage VDD and the first terminal N1, the second transistor T2 is connected between the first terminal N1 and ground GND, the third transistor T3 is connected between the input voltage VDD and the second terminal N2, and the fourth
  - 10 transistor T4 is connected between the second terminal N2 and the output terminal, characterized in that it comprises at least a control circuit for supplying said control signal applied between the gate and the source of one of the transistors T1-T2-T3 functioning as a switch, said control circuit having the particular function of generating a control signal having an amplitude which is inversely proportional to the input voltage VDD when the
  - 15 transistor which it controls is equivalent to a closed switch.
- 
2. A voltage converter as claimed in claim 1, characterized in that said control circuit comprises, when it controls a transistor of the P-MOS type:
    - an additional transistor M1 of the P-MOS type functioning as a closed switch,
  - 20 - a current source IREF\_1 arranged in series with the drain-source junction of said additional transistor M1,
  - a switch COM1 having two inputs, the first input E1 of which is connected to the central tap P of the additional transistor M1 and the current source IREF\_1, and the second input E2 is connected to the input voltage VDD, said switch being controlled via said
  - 25 clock signal.
- 
3. A voltage converter as claimed in claim 1, characterized in that said control circuit comprises, when it controls a transistor of the N-MOS type:
    - an additional transistor M2 of the N-MOS type functioning as a closed switch,

- a current source IREF\_2 arranged in series with the drain-source junction of said additional transistor M2,
- a switch COM2 having two inputs, the first input E1 of which is connected to the central tap P of the additional transistor M2 and the current source IREF\_2, and the second input E2 is connected to ground GND, said switch being controlled via said clock signal.

4. An integrated circuit comprising a voltage converter for generating an output voltage at an output terminal from an input voltage VDD taken from ground GND, said voltage converter comprising:

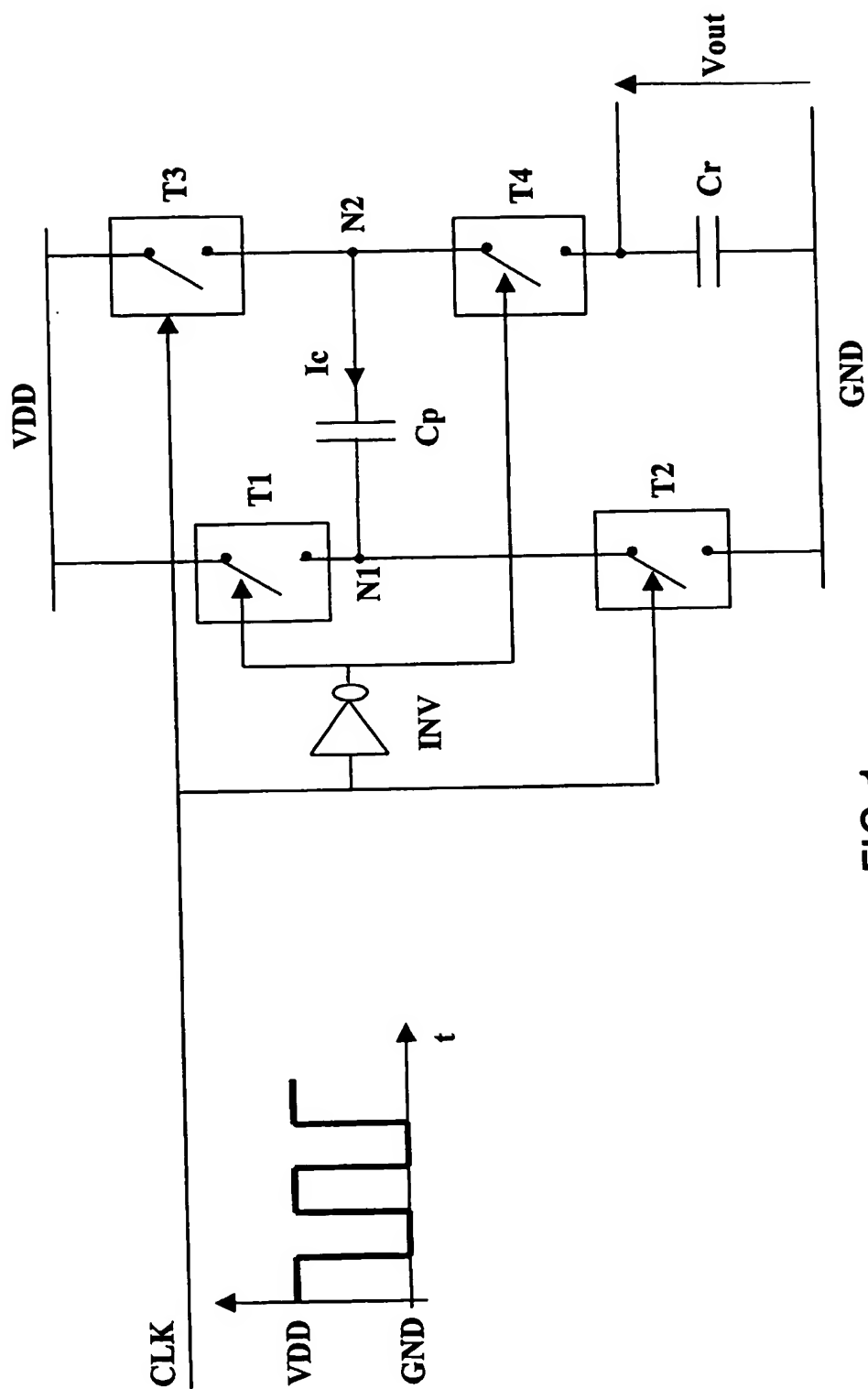
- a capacitance Cp having a first terminal N1 and a second terminal N2,
- four transistors T1-T2-T3-T4 of the MOS type functioning as switches, each transistor being controlled by a control signal having a level varying in the rhythm of a clock signal, each transistor comprising a source, a gate, a drain, and such that the first transistor T1 is connected between the input voltage VDD and the first terminal N1, the second transistor T2 is connected between the first terminal N1 and ground GND, the third transistor T3 is connected between the input voltage VDD and the second terminal N2, and the fourth transistor T4 is connected between the second terminal N2 and the output terminal, characterized in that the voltage converter comprises at least a control circuit for supplying said control signal applied between the gate and the source of one of the transistors T1-T2-T3 functioning as a switch, said control signal having the particular function of generating a control signal having an amplitude which is inversely proportional to the input voltage VDD when the transistor which it controls is equivalent to a closed switch.

5. A device for reading smart cards, comprising a voltage converter for generating an output voltage at an output terminal from an input voltage VDD taken from ground GND, said voltage converter comprising:

- a capacitance Cp having a first terminal N1 and a second terminal N2,
- four transistors T1-T2-T3-T4 of the MOS type functioning as switches, each transistor being controlled by a control signal having a level varying in the rhythm of a clock signal, each transistor comprising a source, a gate, a drain, and such that the first transistor T1 is connected between the input voltage VDD and the first terminal N1, the second transistor T2 is connected between the first terminal N1 and ground GND, the third transistor T3 is

connected between the input voltage VDD and the second terminal N2, and the fourth transistor T4 is connected between the second terminal N2 and the output terminal, characterized in that the voltage converter comprises at least a control circuit for supplying said control signal applied between the gate and the source of one of the transistors T1-T2-T3

5 functioning as a switch, said control signal having the particular function of generating a control signal with an amplitude which is inversely proportional to the input voltage VDD when the transistor which it controls is equivalent to a closed switch.



**FIG. 1**

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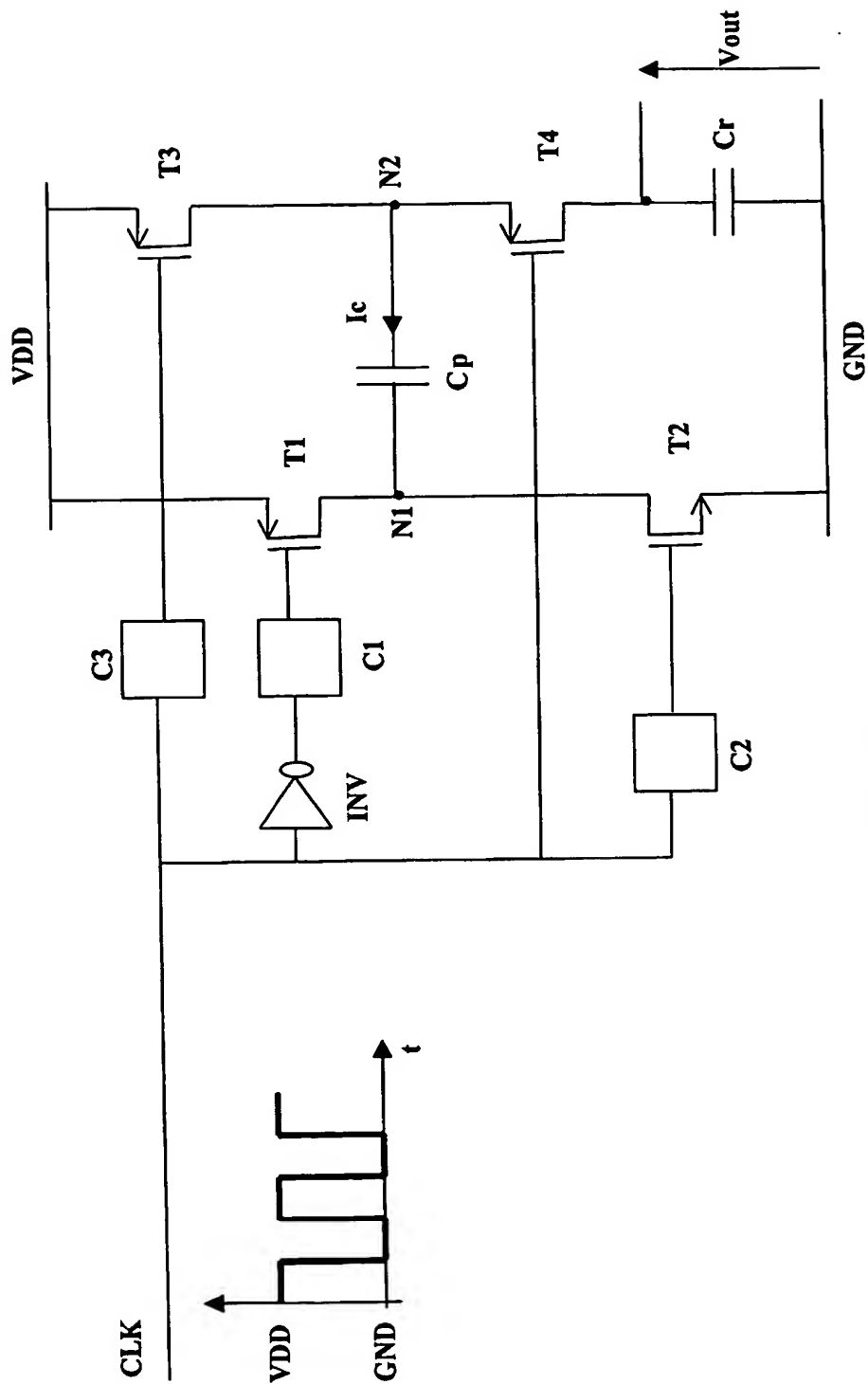


FIG.2

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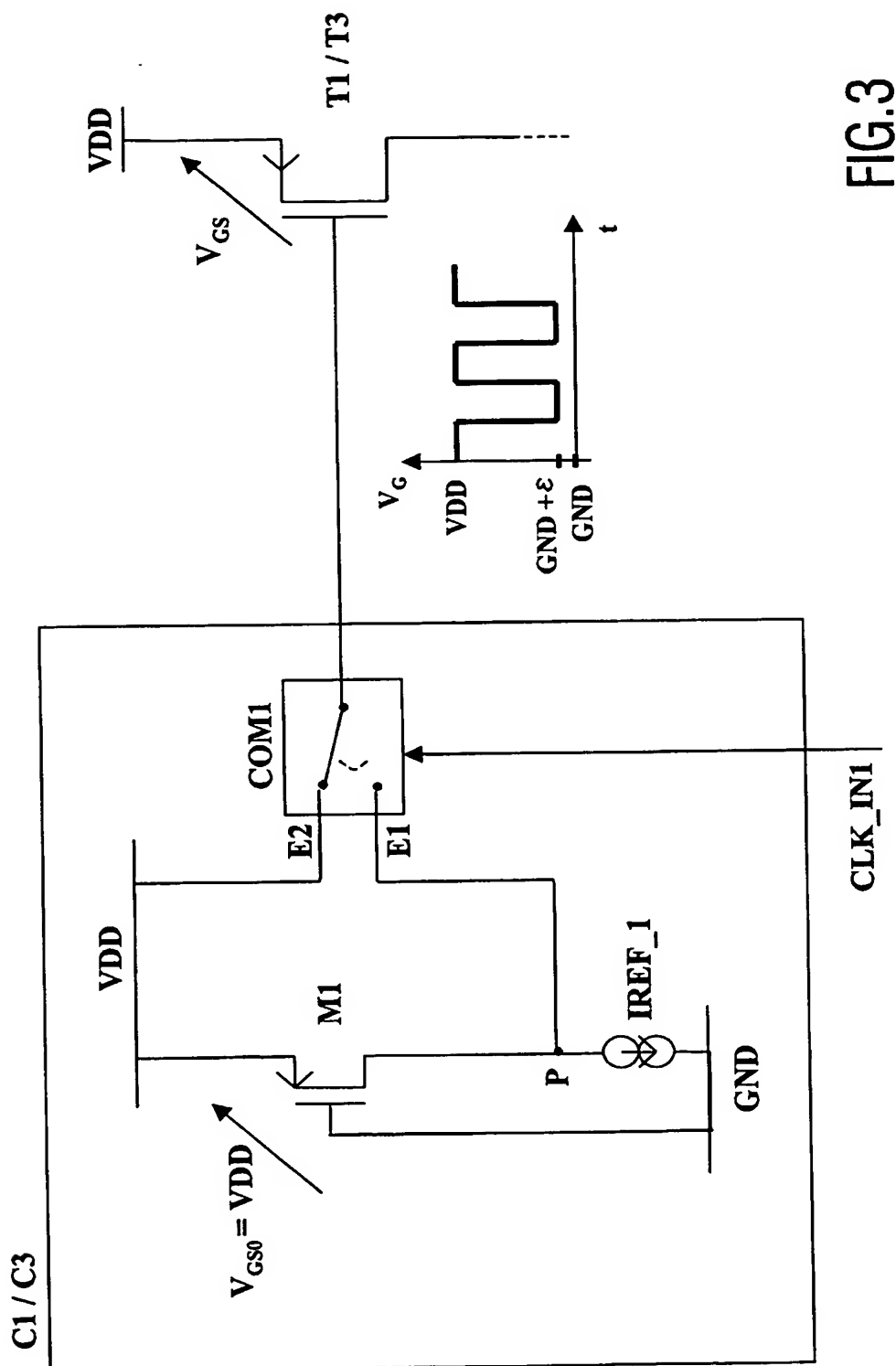


FIG.3



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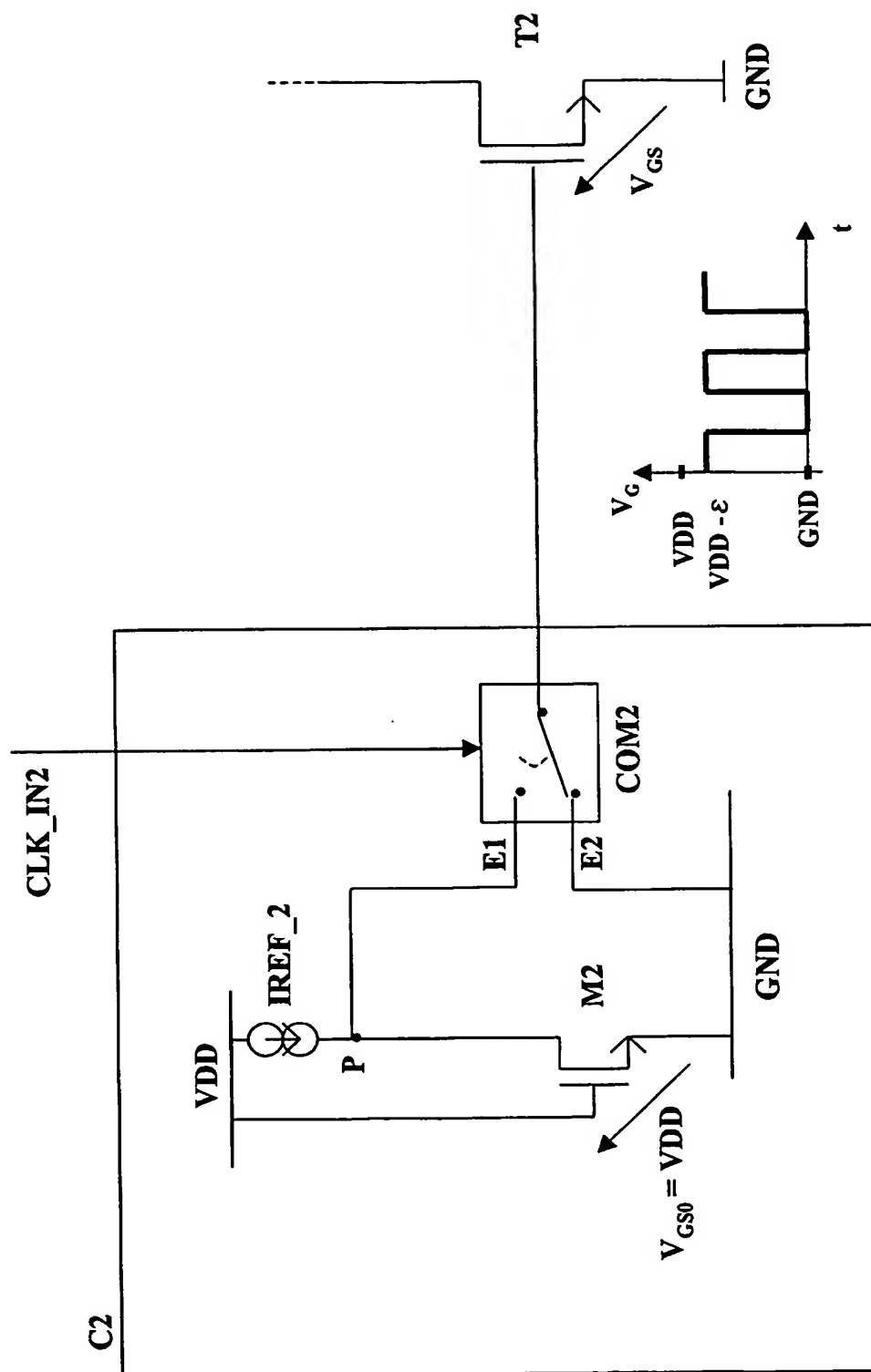


FIG.4

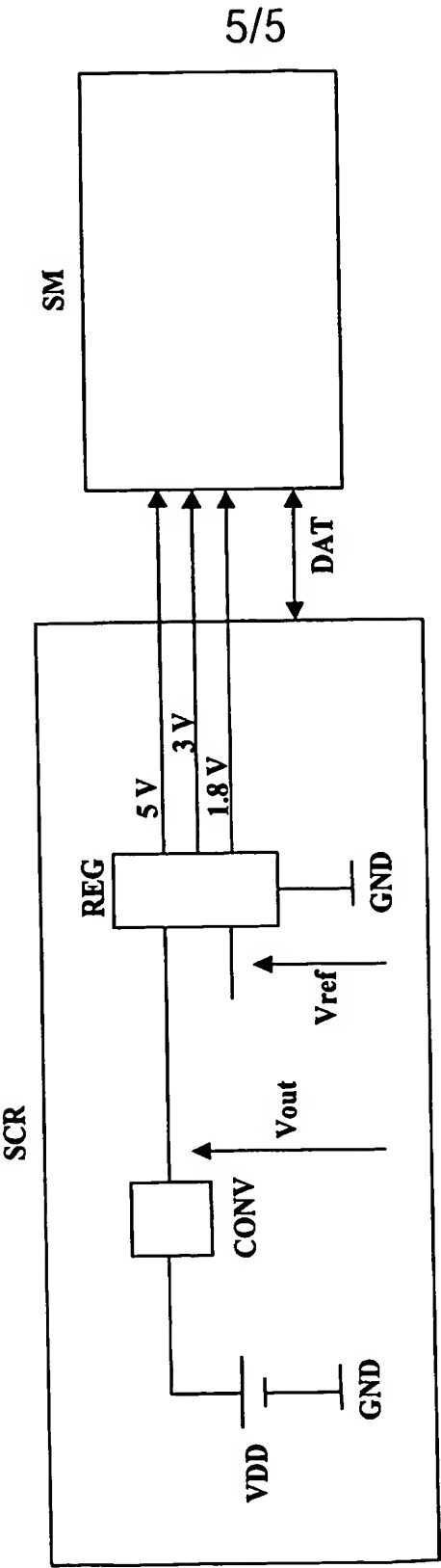


FIG.5

# INTERNATIONAL SEARCH REPORT

PCT/TB 03/01026

<b>A. CLASSIFICATION OF SUBJECT MATTER</b> IPC 7    H02M3/07    H03K17/16		
According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b> Minimum documentation searched (classification system followed by classification symbols) IPC 7    H02M    H03K		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the International search (name of data base and, where practical, search terms used) EPO-Internal, WPI Data		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 233 238 A (MATTOS DERWIN W) 3 August 1993 (1993-08-03) the whole document ---	1-5
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<div style="display: flex; justify-content: space-between;"> <span><input checked="" type="checkbox"/> Further documents are listed in the continuation of box C.</span> <span><input checked="" type="checkbox"/> Patent family members are listed in annex.</span> </div>		
<div style="display: flex;"> <div style="flex: 1;"> <p>* Special categories of cited documents:</p> <p>*A* document defining the general state of the art which is not considered to be of particular relevance</p> <p>*E* earlier document but published on or after the International filing date</p> <p>*L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>*O* document referring to an oral disclosure, use, exhibition or other means</p> <p>*P* document published prior to the International filing date but later than the priority date claimed</p> </div> <div style="flex: 1;"> <p>*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>*Z* document member of the same patent family</p> </div> </div>		
Date of the actual completion of the international search  <div style="text-align: center; font-weight: bold;">28 August 2003</div>		Date of mailing of the international search report  <div style="text-align: center; font-weight: bold;">03/09/2003</div>
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016		Authorized officer  <div style="text-align: center; font-weight: bold;">Thisse, S</div>

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